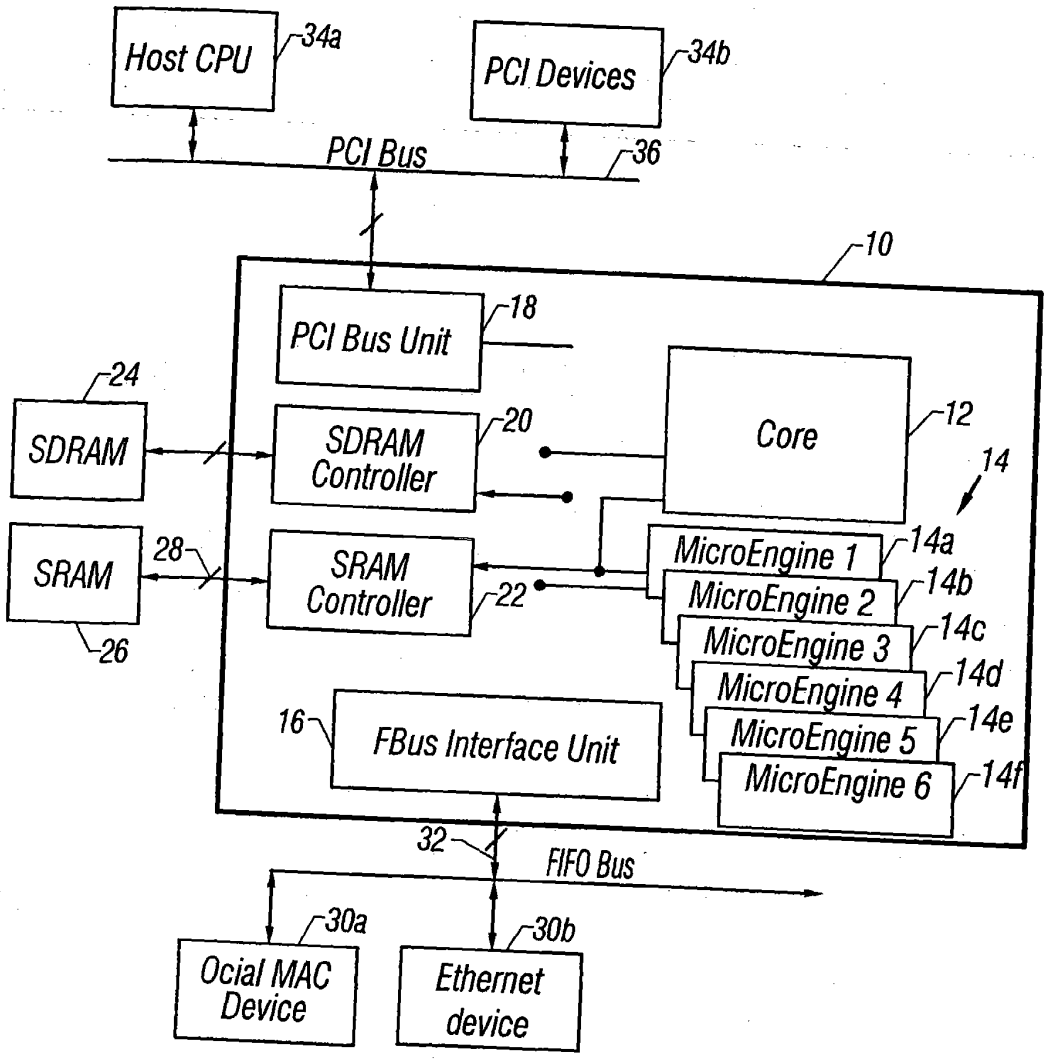
Host CPU
34a
PCI Devices
34b
PCI Bus
36
10
PCI Bus Unit
18
24
SDRAM
SDRAM Controller
20
Core
12
14
SRAM
28
SRAM Controller
22
MicroEngine 1
14a
MicroEngine 2
14b
MicroEngine 3
14c
MicroEngine 4
14d
MicroEngine 5
14e
MicroEngine 6
14f
26
16
FBus Interface Unit
32
FIFO Bus
30a
30b
Ocial MAC Device
Ethernet device

FIG. 1

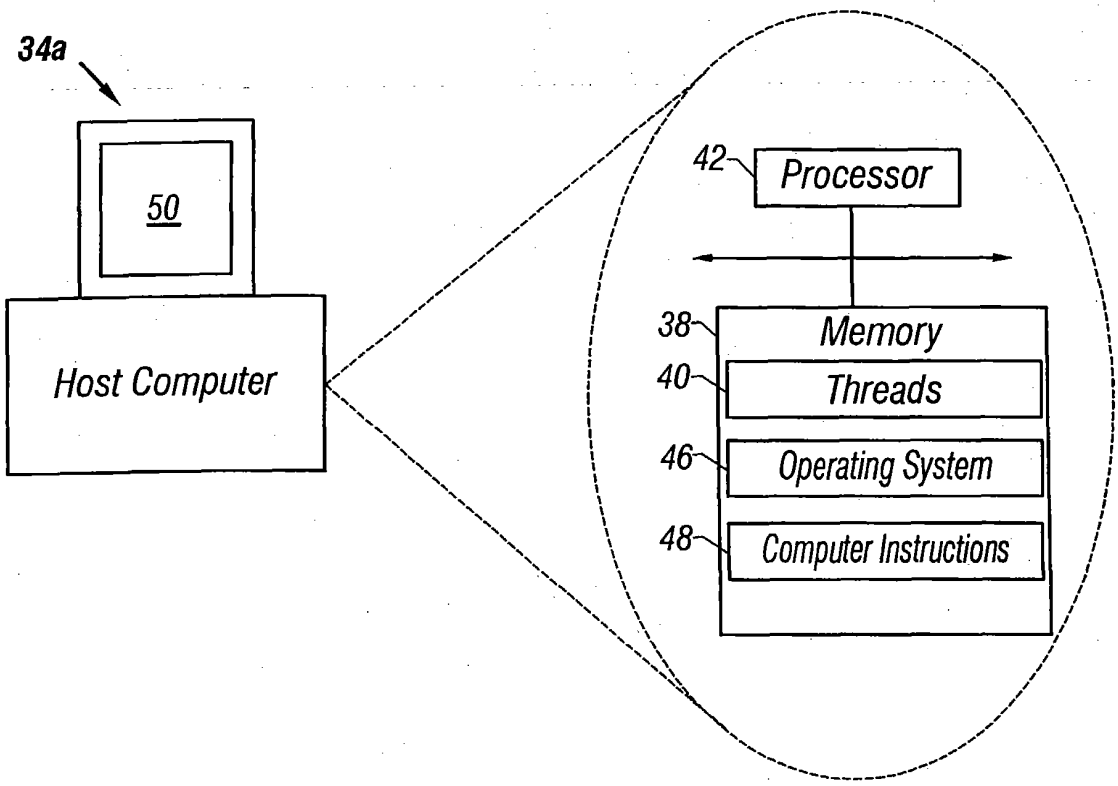
34a
50
Host Computer
42
Processor
38
Memory
40
Threads
46
Operating System
48
Computer Instructions

FIG. 2

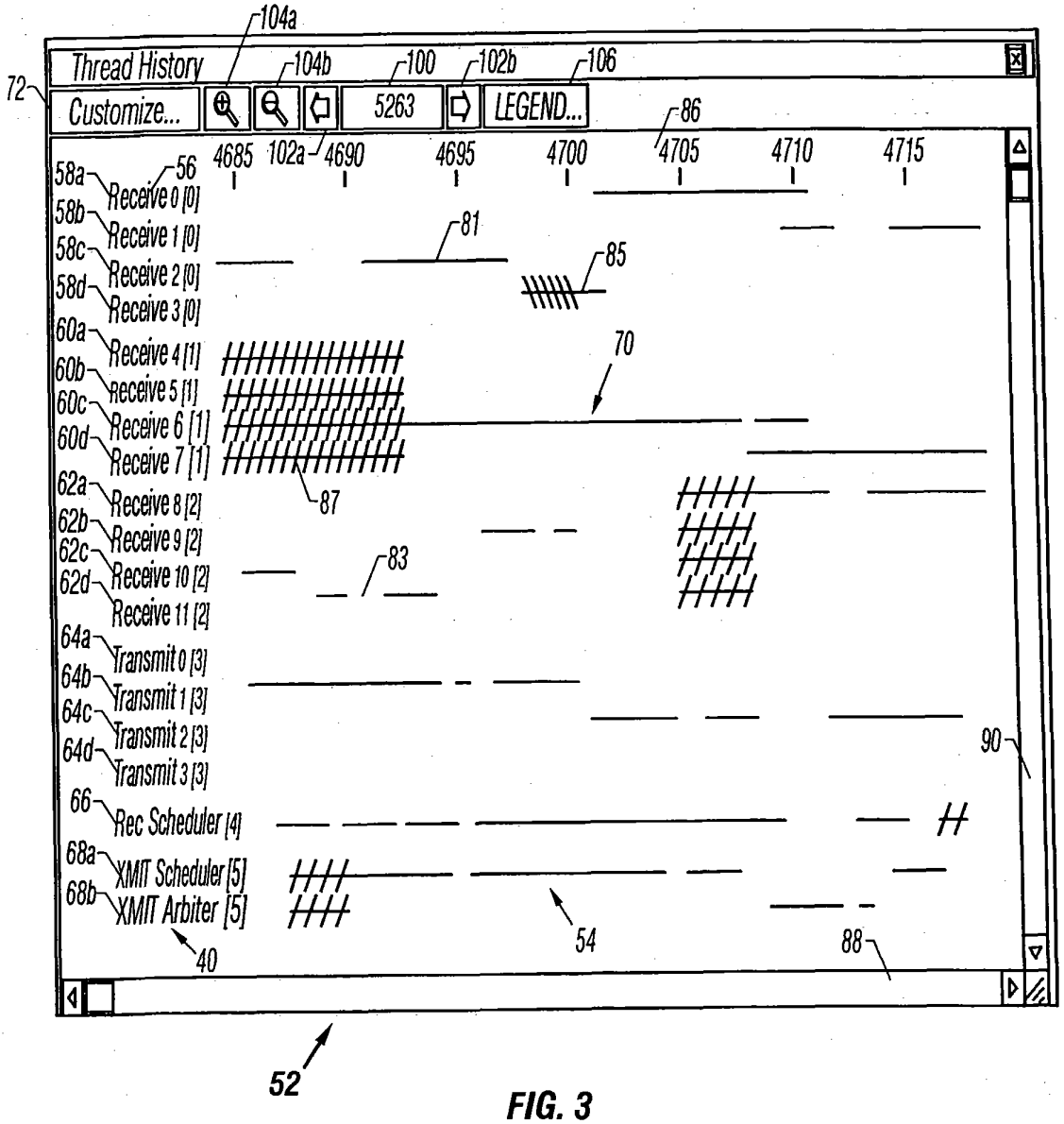
104a
Thread History
104b
100
102b
106
72
Customize...
5263
LEGEND...
86
4685
102a
4690
4695
4700
4705
4710
4715
56
58a Receive 0 [0]
58b Receive 1 [0]
58c Receive 2 [0]
58d Receive 3 [0]
60a Receive 4 [1]
60b receive 5 [1]
60c Receive 6 [1]
60d Receive 7 [1]
62a Receive 8 [2]
62b Receive 9 [2]
62c Receive 10 [2]
62d Receive 11 [2]
64a Transmit 0 [3]
64b Transmit 1 [3]
64c Transmit 2 [3]
64d Transmit 3 [3]
66 Rec Scheduler [4]
68a XMIT Scheduler [5]
68b XMIT Arbiter [5]
81
85
70
87
83
90
54
88
40
52

FIG. 3

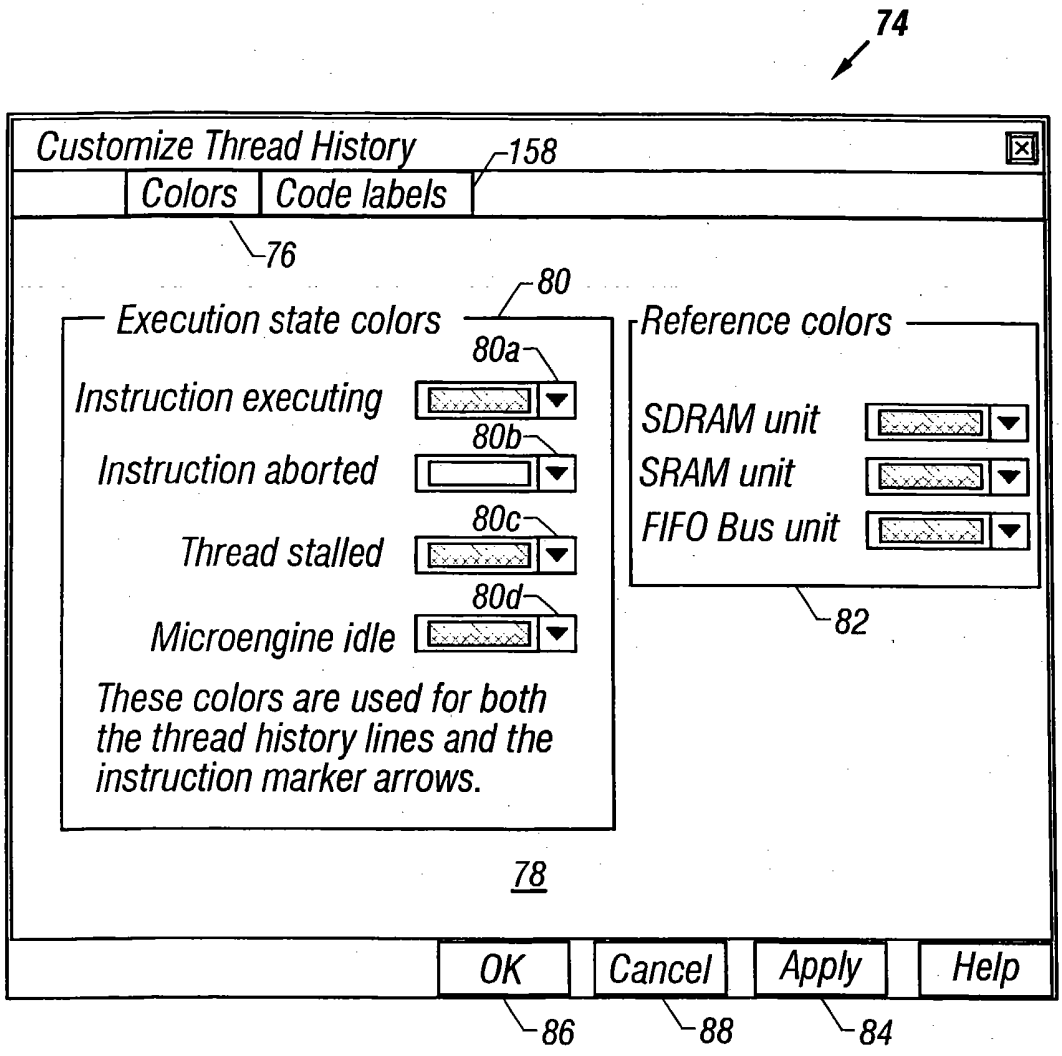
74
Customize Thread History
158
Colors
Code labels
76
80
Execution state colors
80a
Instruction executing
80b
Instruction aborted
80c
Thread stalled
80d
Microengine idle
These colors are used for both the thread history lines and the instruction marker arrows.
Reference colors
SDRAM unit
SRAM unit
FIFO Bus unit
82
78
OK
Cancel
Apply
Help
86
88
84

**FIG. 4**

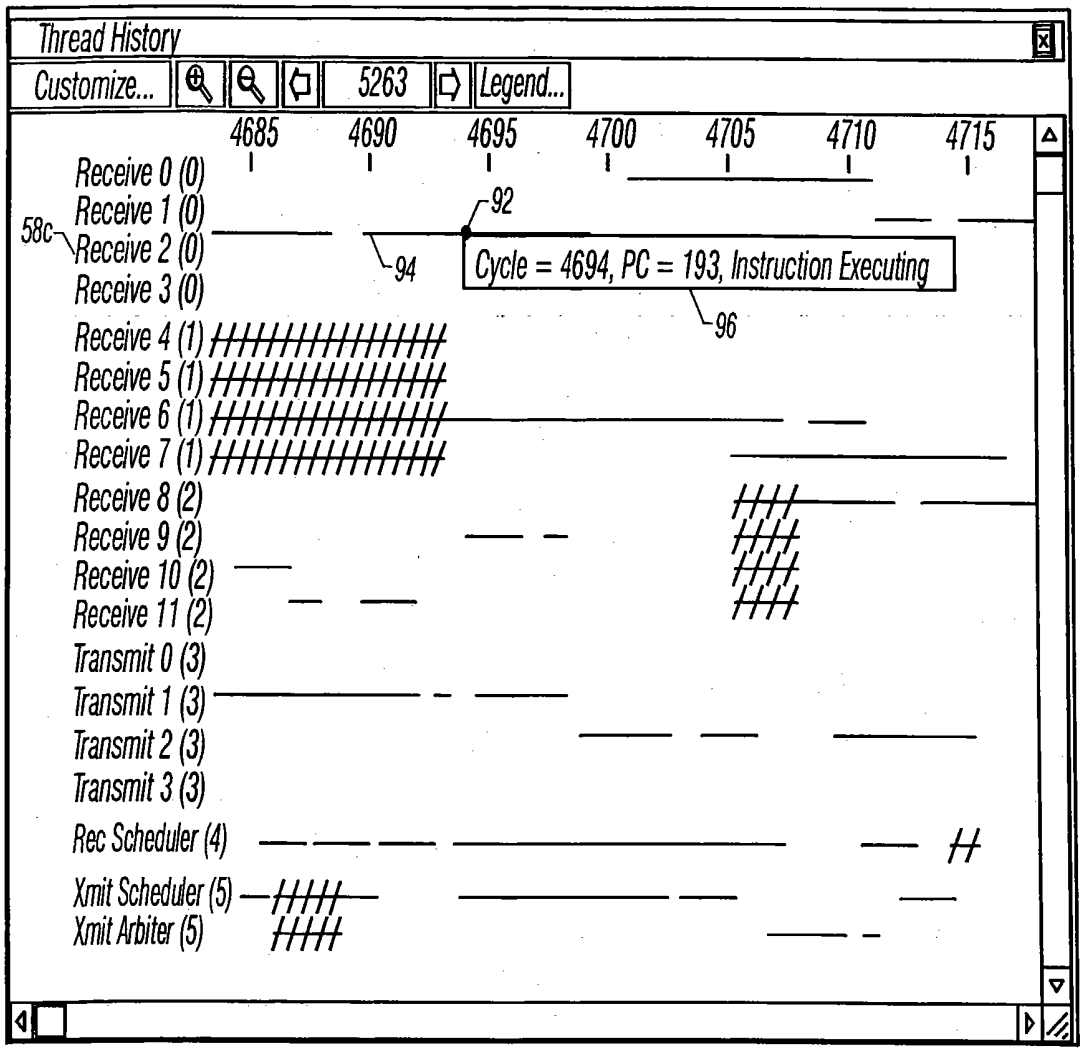
Thread History
Customize...
5263
Legend...
4685
4690
4695
4700
4705
4710
4715
Receive 0 (0)
Receive 1 (0)
Receive 2 (0)
Receive 3 (0)
Receive 4 (1)
Receive 5 (1)
Receive 6 (1)
Receive 7 (1)
Receive 8 (2)
Receive 9 (2)
Receive 10 (2)
Receive 11 (2)
Transmit 0 (3)
Transmit 1 (3)
Transmit 2 (3)
Transmit 3 (3)
Rec Scheduler (4)
Xmit Scheduler (5)
Xmit Arbiter (5)
58c
92
94
Cycle = 4694, PC = 193, Instruction Executing
96
52

FIG. 5

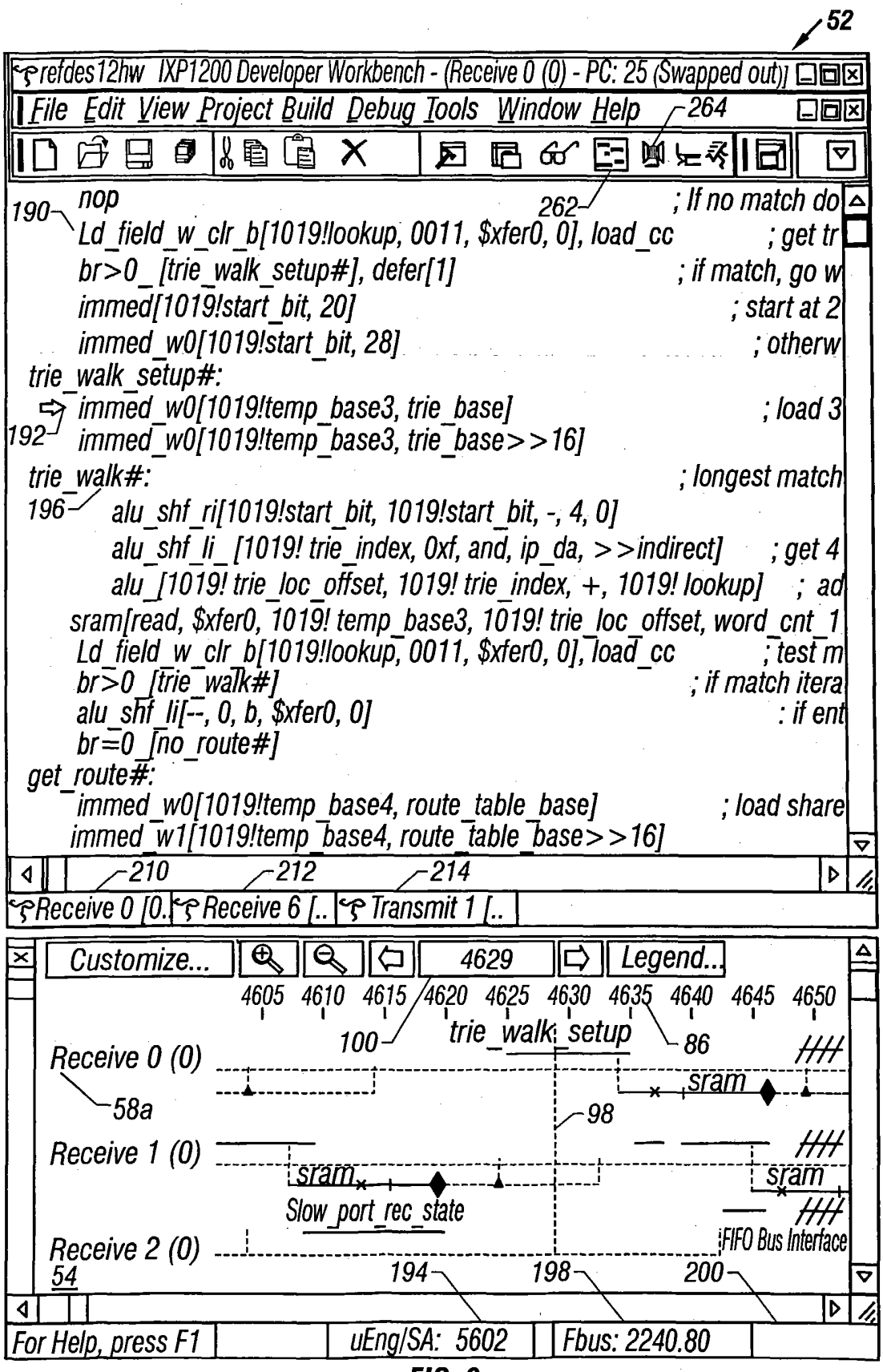
52
refdes12hw IXP1200 Developer Workbench - (Receive 0 (0) - PC: 25 (Swapped out))
File Edit View Project Build Debug Tools Window Help
264
262
190
192
196
nop ; If no match do
Ld_field_w_clr_b[1019!lookup, 0011, $xfer0, 0], load_cc ; get tr
br>0_[trie_walk_setup#], defer[1] ; if match, go w
immed[1019!start_bit, 20] ; start at 2
immed_w0[1019!start_bit, 28] ; otherw
trie_walk_setup#:
immed_w0[1019!temp_base3, trie_base] ; load 3
immed_w0[1019!temp_base3, trie_base>>16]
trie_walk#: ; longest match
alu_shf_ri[1019!start_bit, 1019!start_bit, -, 4, 0]
alu_shf_li_[1019! trie_index, 0xf, and, ip_da, >>indirect] ; get 4
alu_[1019! trie_loc_offset, 1019! trie_index, +, 1019! lookup] ; ad
sram[read, $xfer0, 1019! temp_base3, 1019! trie_loc_offset, word_cnt_1
Ld_field_w_clr_b[1019!lookup, 0011, $xfer0, 0], load_cc ; test m
br>0_[trie_walk#] ; if match itera
alu_shf_li[--, 0, b, $xfer0, 0] ; if ent
br=0_[no_route#]
get_route#:
immed_w0[1019!temp_base4, route_table_base] ; load share
immed_w1[1019!temp_base4, route_table_base>>16]
210
212
214
Receive 0 [0.
Receive 6 [..
Transmit 1 [..
Customize...
4629
Legend...
4605 4610 4615 4620 4625 4630 4635 4640 4645 4650
100
trie_walk_setup
86
Receive 0 (0)
sram
58a
98
Receive 1 (0)
sram
sram
Slow_port_rec_state
Receive 2 (0)
FIFO Bus Interface
54
194
198
200
For Help, press F1
uEng/SA: 5602
Fbus: 2240.80

**FIG. 6**

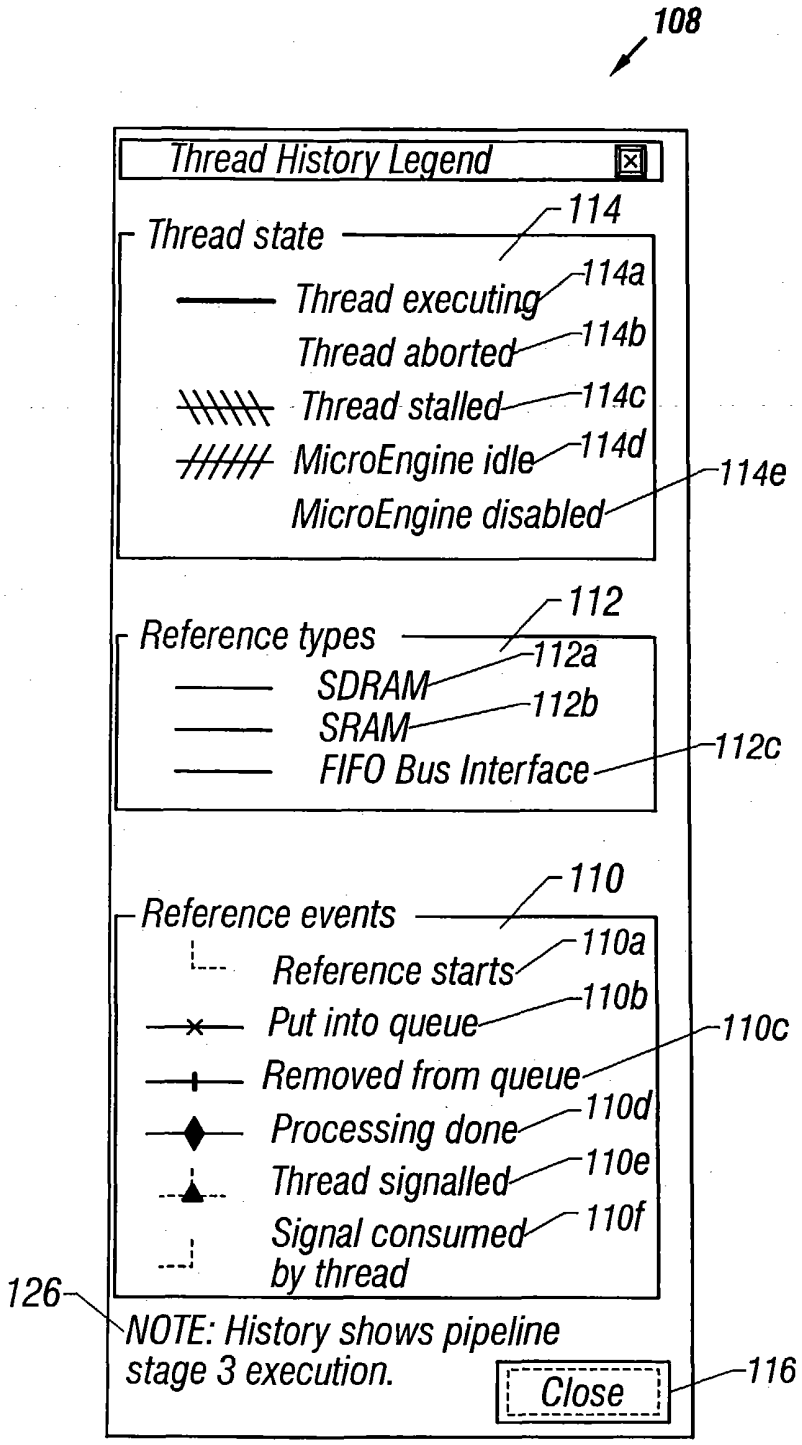
108
Thread History Legend
Thread state
114
Thread executing
114a
Thread aborted
114b
Thread stalled
114c
MicroEngine idle
114d
MicroEngine disabled
114e
Reference types
112
SDRAM
112a
SRAM
112b
FIFO Bus Interface
112c
Reference events
110
Reference starts
110a
Put into queue
110b
Removed from queue
110c
Processing done
110d
Thread signalled
110e
Signal consumed by thread
110f
126
NOTE: History shows pipeline stage 3 execution.
Close
116

FIG. 7

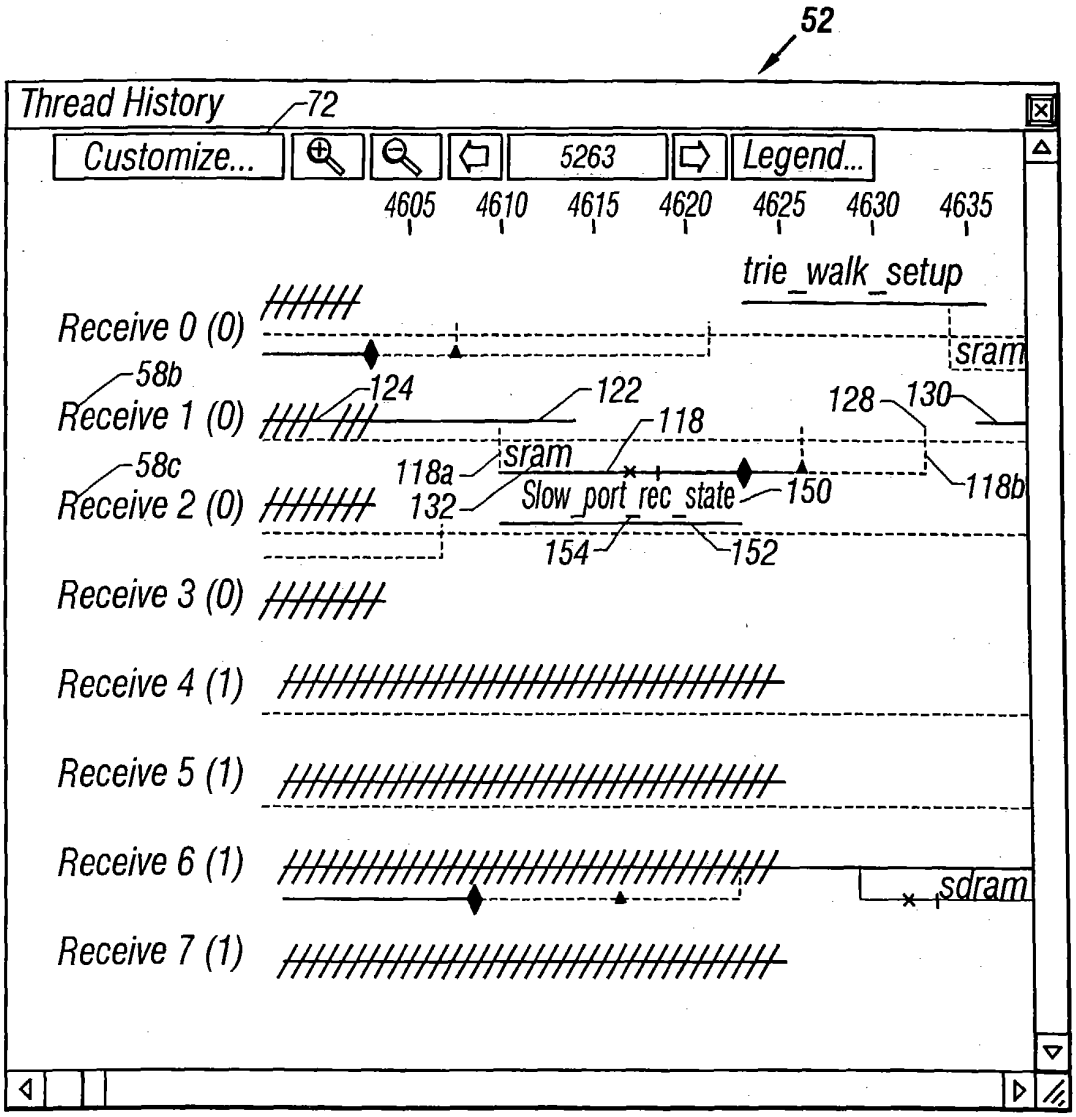
52
Thread History
72
Customize...
5263
Legend...
4605
4610
4615
4620
4625
4630
4635
trie_walk_setup
Receive 0 (0)
sram
58b
Receive 1 (0)
124
122
128
130
118
sram
58c
Receive 2 (0)
118a
132
Slow_port_rec_state
150
118b
154
152
Receive 3 (0)
Receive 4 (1)
Receive 5 (1)
Receive 6 (1)
sdram
Receive 7 (1)

FIG. 8

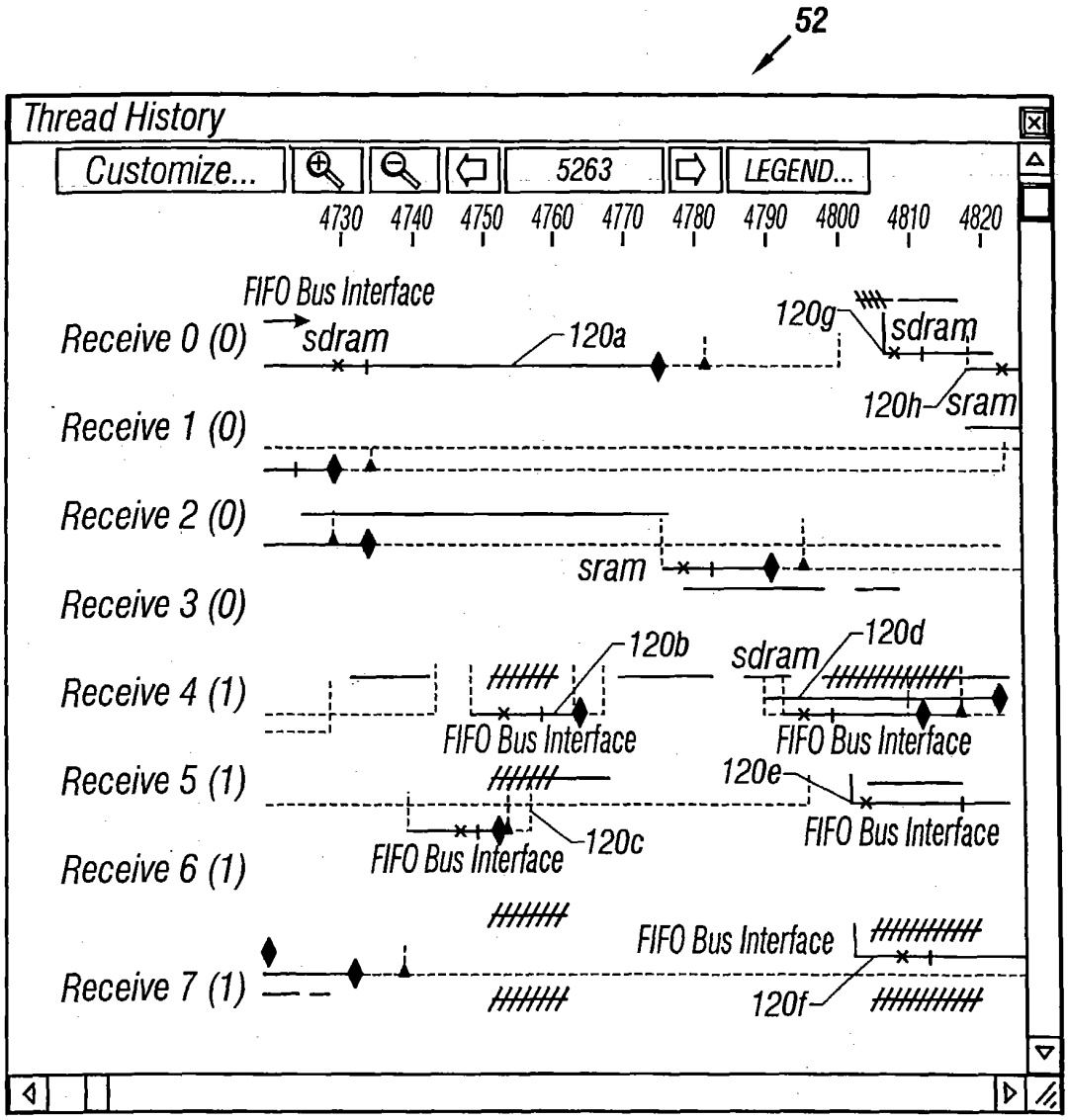
52
Thread History
Customize...
5263
LEGEND...
4730
4740
4750
4760
4770
4780
4790
4800
4810
4820
FIFO Bus Interface
Receive 0 (0)
sdram
120a
120g
sdram
120h
sram
Receive 1 (0)
Receive 2 (0)
sram
Receive 3 (0)
120b
sdram
120d
Receive 4 (1)
FIFO Bus Interface
FIFO Bus Interface
Receive 5 (1)
120e
FIFO Bus Interface
120c
FIFO Bus Interface
Receive 6 (1)
FIFO Bus Interface
Receive 7 (1)
120f

FIG. 9

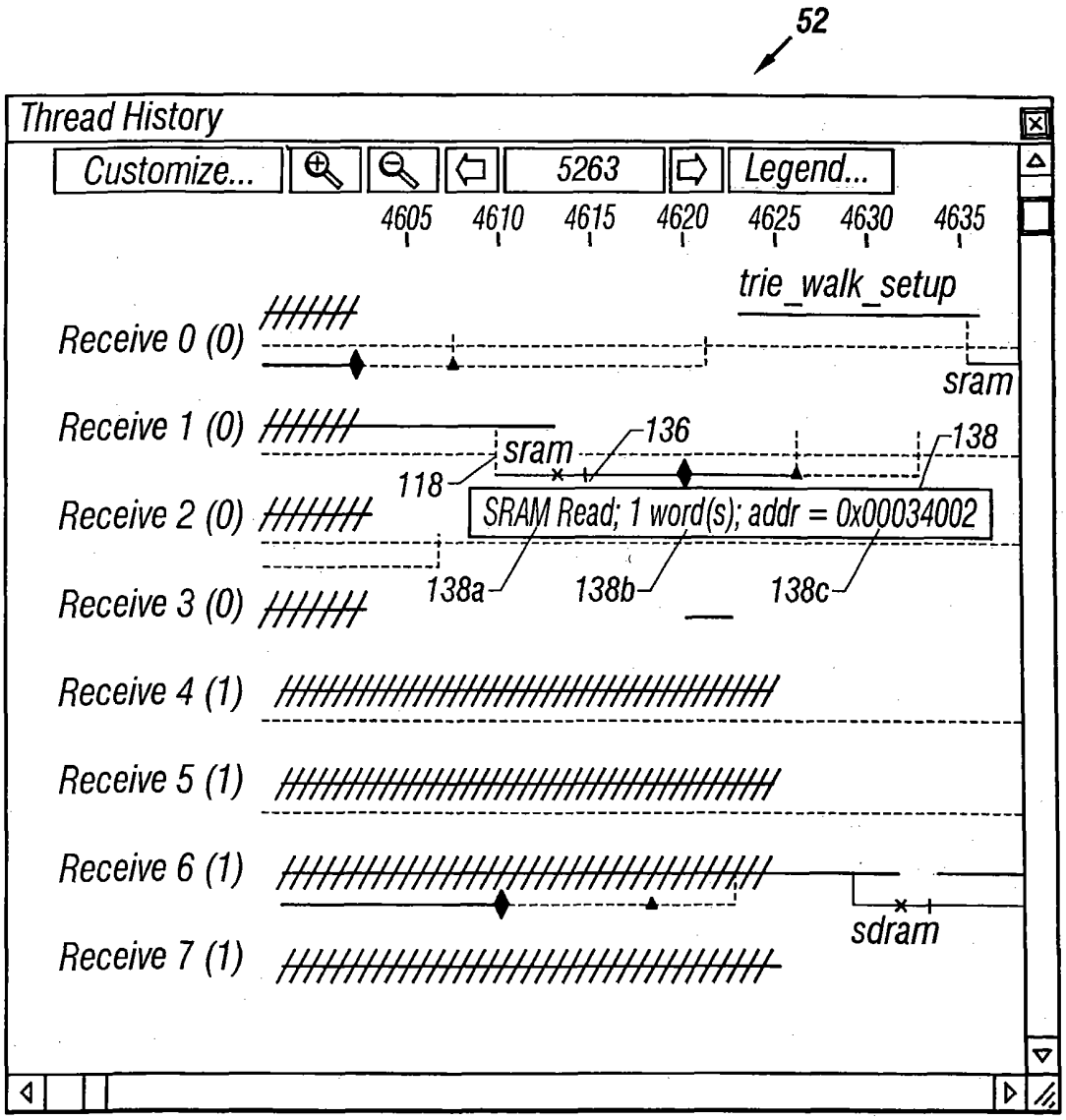
52
Thread History
Customize...
5263
Legend...
4605
4610
4615
4620
4625
4630
4635
trie_walk_setup
Receive 0 (0)
sram
Receive 1 (0)
sram
136
138
118
Receive 2 (0)
SRAM Read; 1 word(s); addr = 0x00034002
138a
138b
138c
Receive 3 (0)
Receive 4 (1)
Receive 5 (1)
Receive 6 (1)
sdram
Receive 7 (1)

FIG. 10

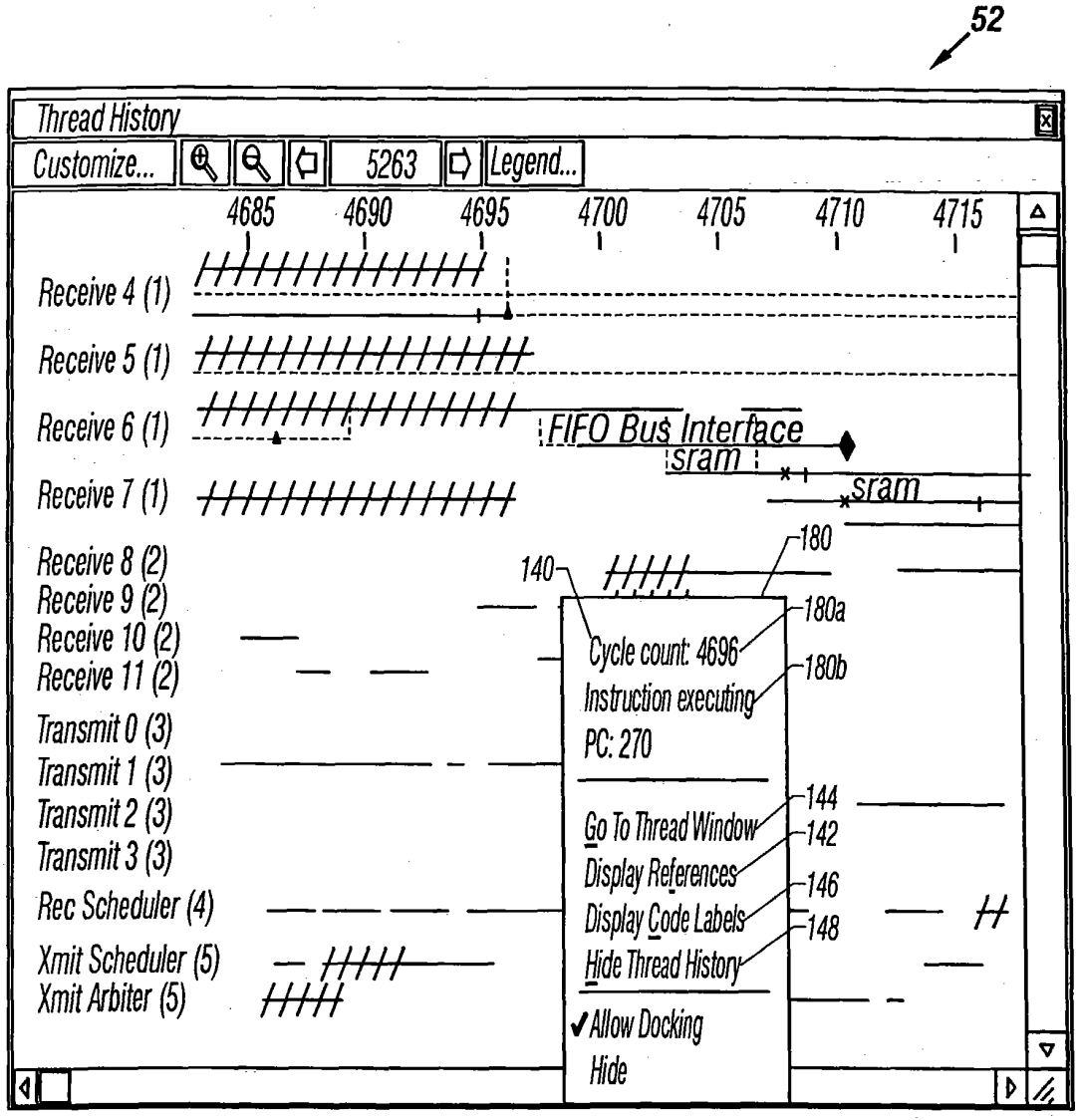
52
Thread History
Customize...
5263
Legend...
4685
4690
4695
4700
4705
4710
4715
Receive 4 (1)
Receive 5 (1)
Receive 6 (1)
Receive 7 (1)
Receive 8 (2)
Receive 9 (2)
Receive 10 (2)
Receive 11 (2)
Transmit 0 (3)
Transmit 1 (3)
Transmit 2 (3)
Transmit 3 (3)
Rec Scheduler (4)
Xmit Scheduler (5)
Xmit Arbiter (5)
FIFO Bus Interface
sram
sram
140
180
180a
180b
Cycle count: 4696
Instruction executing
PC: 270
Go To Thread Window
Display References
Display Code Labels
Hide Thread History
Allow Docking
Hide
144
142
146
148

FIG. 11

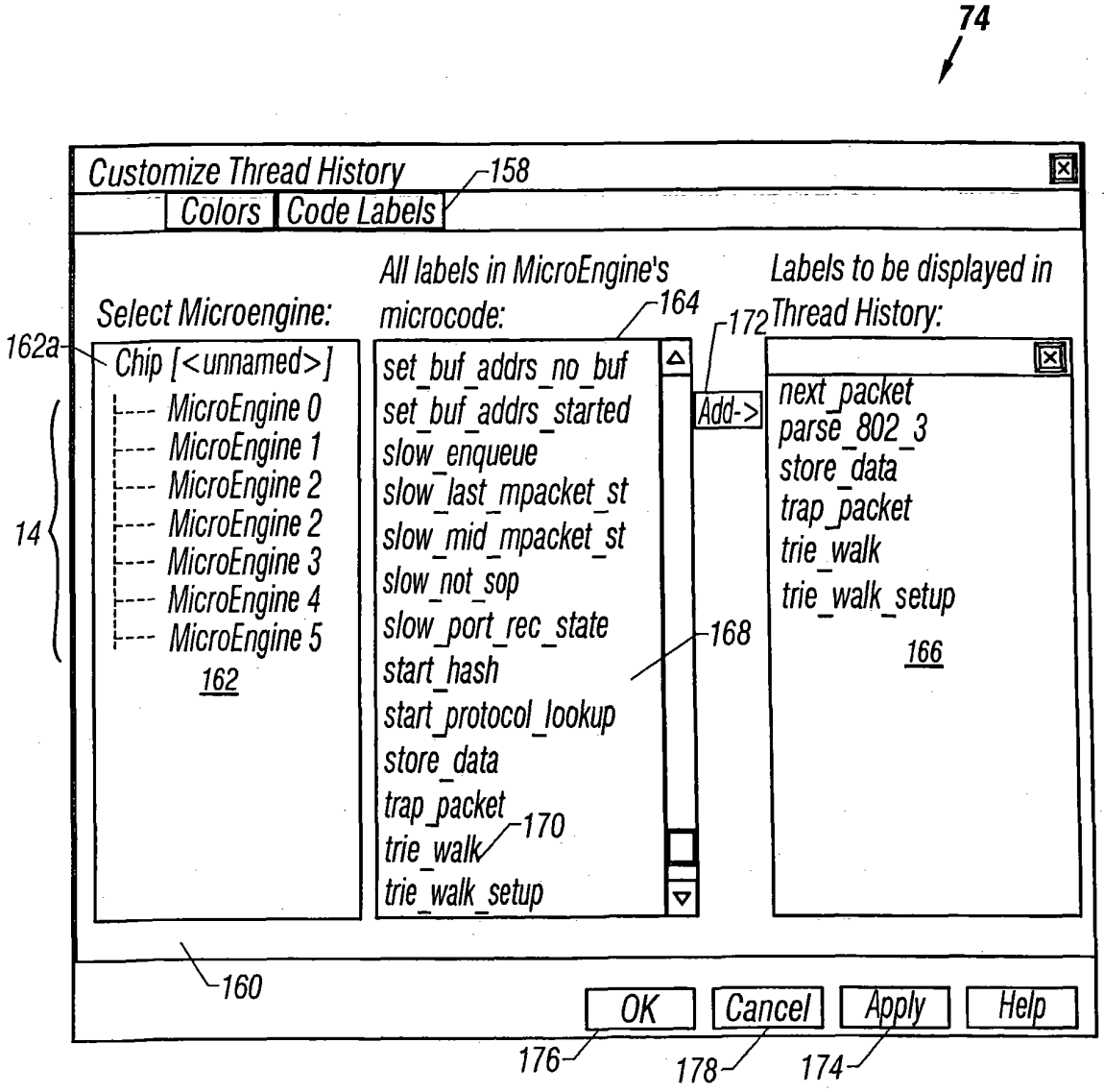
74
Customize Thread History
158
Colors
Code Labels
Select Microengine:
All labels in MicroEngine's microcode:
164
Labels to be displayed in Thread History:
172
162a
Chip [<unnamed>]
MicroEngine 0
MicroEngine 1
MicroEngine 2
MicroEngine 2
MicroEngine 3
MicroEngine 4
MicroEngine 5
162
14
set_buf_addrs_no_buf
set_buf_addrs_started
slow_enqueue
slow_last_mpacket_st
slow_mid_mpacket_st
slow_not_sop
slow_port_rec_state
start_hash
start_protocol_lookup
store_data
trap_packet
trie_walk
trie_walk_setup
170
168
Add->
next_packet
parse_802_3
store_data
trap_packet
trie_walk
trie_walk_setup
166
160
OK
Cancel
Apply
Help
176
178
174

FIG. 12

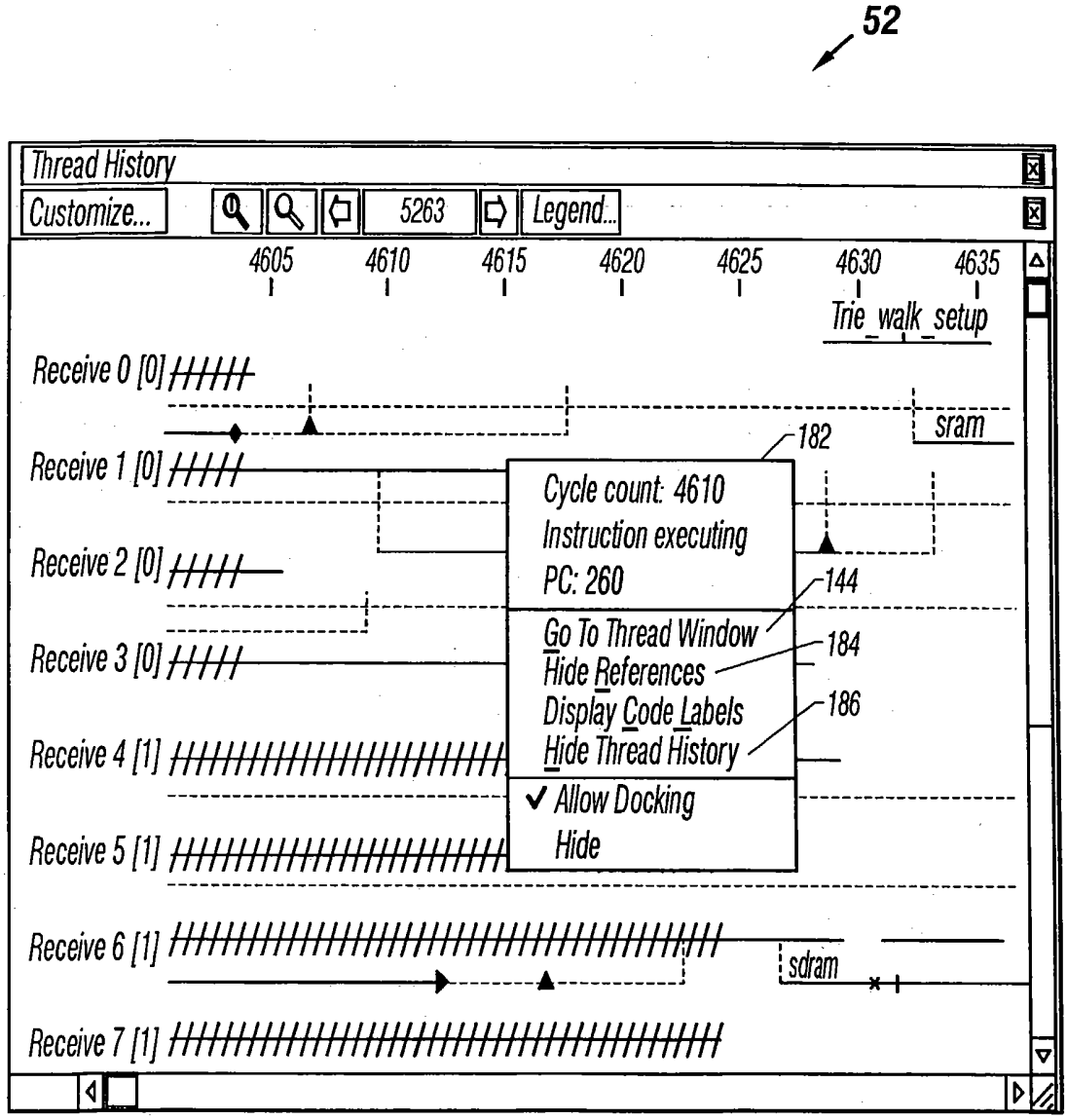
52
Thread History
Customize...
5263
Legend...
4605
4610
4615
4620
4625
4630
4635
Trie_walk_setup
Receive 0 [0]
Receive 1 [0]
Receive 2 [0]
Receive 3 [0]
Receive 4 [1]
Receive 5 [1]
Receive 6 [1]
Receive 7 [1]
sram
sdram
182
Cycle count: 4610
Instruction executing
PC: 260
144
Go To Thread Window
Hide References
184
Display Code Labels
186
Hide Thread History
✓ Allow Docking
Hide

FIG. 13

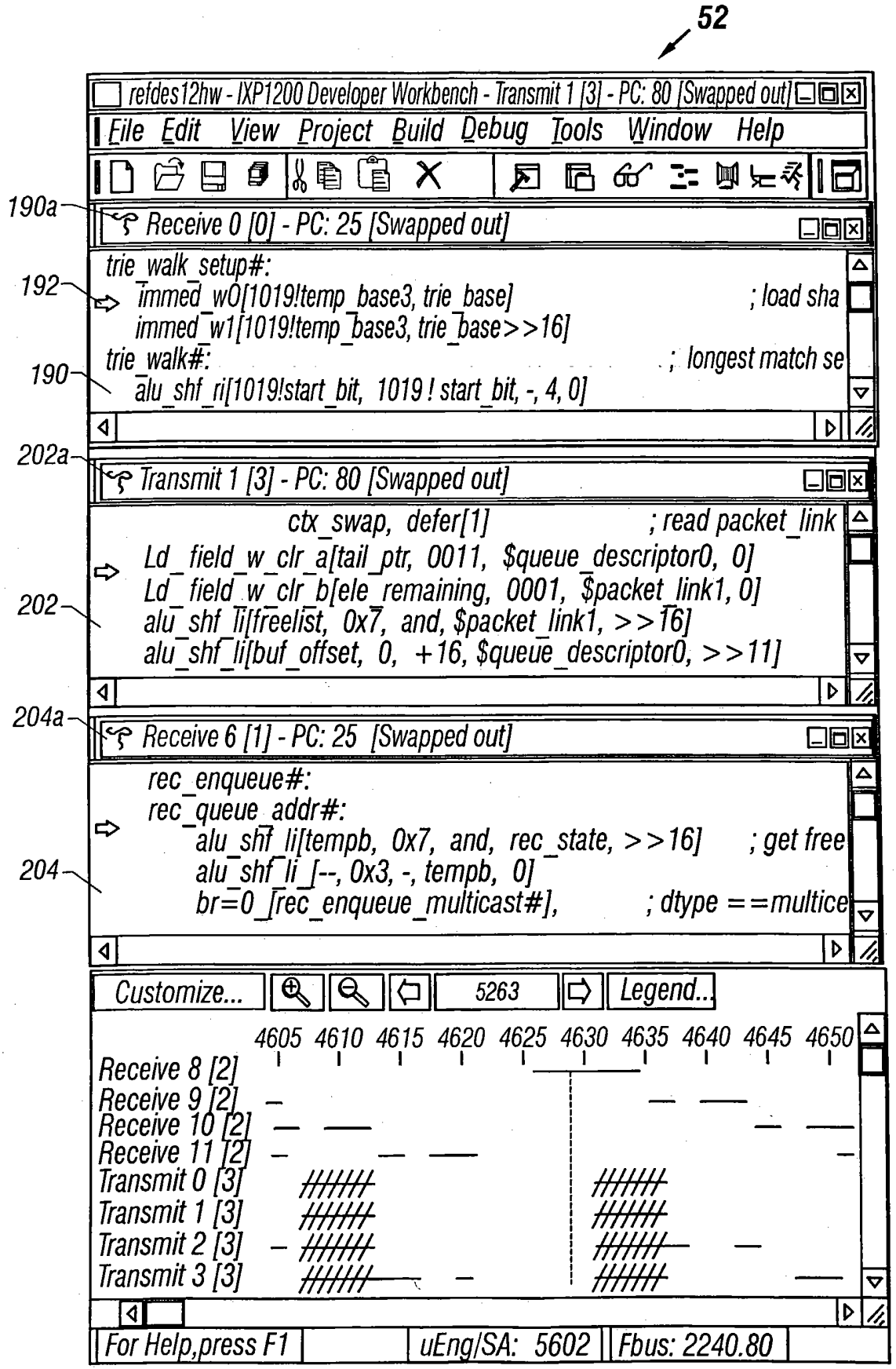
52
refdes12hw - IXP1200 Developer Workbench - Transmit 1 [3] - PC: 80 [Swapped out]
File Edit View Project Build Debug Tools Window Help
190a
Receive 0 [0] - PC: 25 [Swapped out]
trie_walk_setup#:
192
immed_w0[1019!temp_base3, trie_base] ; load sha
immed_w1[1019!temp_base3, trie_base>>16]
trie_walk#: ; longest match se
190
alu_shf_ri[1019!start_bit, 1019 ! start_bit, -, 4, 0]
202a
Transmit 1 [3] - PC: 80 [Swapped out]
ctx_swap, defer[1] ; read packet_link
Ld_field_w_clr_a[tail_ptr, 0011, $queue_descriptor0, 0]
Ld_field_w_clr_b[ele_remaining, 0001, $packet_link1, 0]
202
alu_shf_li[freelist, 0x7, and, $packet_link1, >>16]
alu_shf_li[buf_offset, 0, +16, $queue_descriptor0, >>11]
204a
Receive 6 [1] - PC: 25 [Swapped out]
rec_enqueue#:
rec_queue_addr#:
alu_shf_li[tempb, 0x7, and, rec_state, >>16] ; get free
204
alu_shf_li_[--, 0x3, -, tempb, 0]
br=0_[rec_enqueue_multicast#], ; dtype ==multice
Customize...
5263
Legend..
4605 4610 4615 4620 4625 4630 4635 4640 4645 4650
Receive 8 [2]
Receive 9 [2]
Receive 10 [2]
Receive 11 [2]
Transmit 0 [3]
Transmit 1 [3]
Transmit 2 [3]
Transmit 3 [3]
For Help,press F1
uEng/SA: 5602
Fbus: 2240.80

FIG. 14

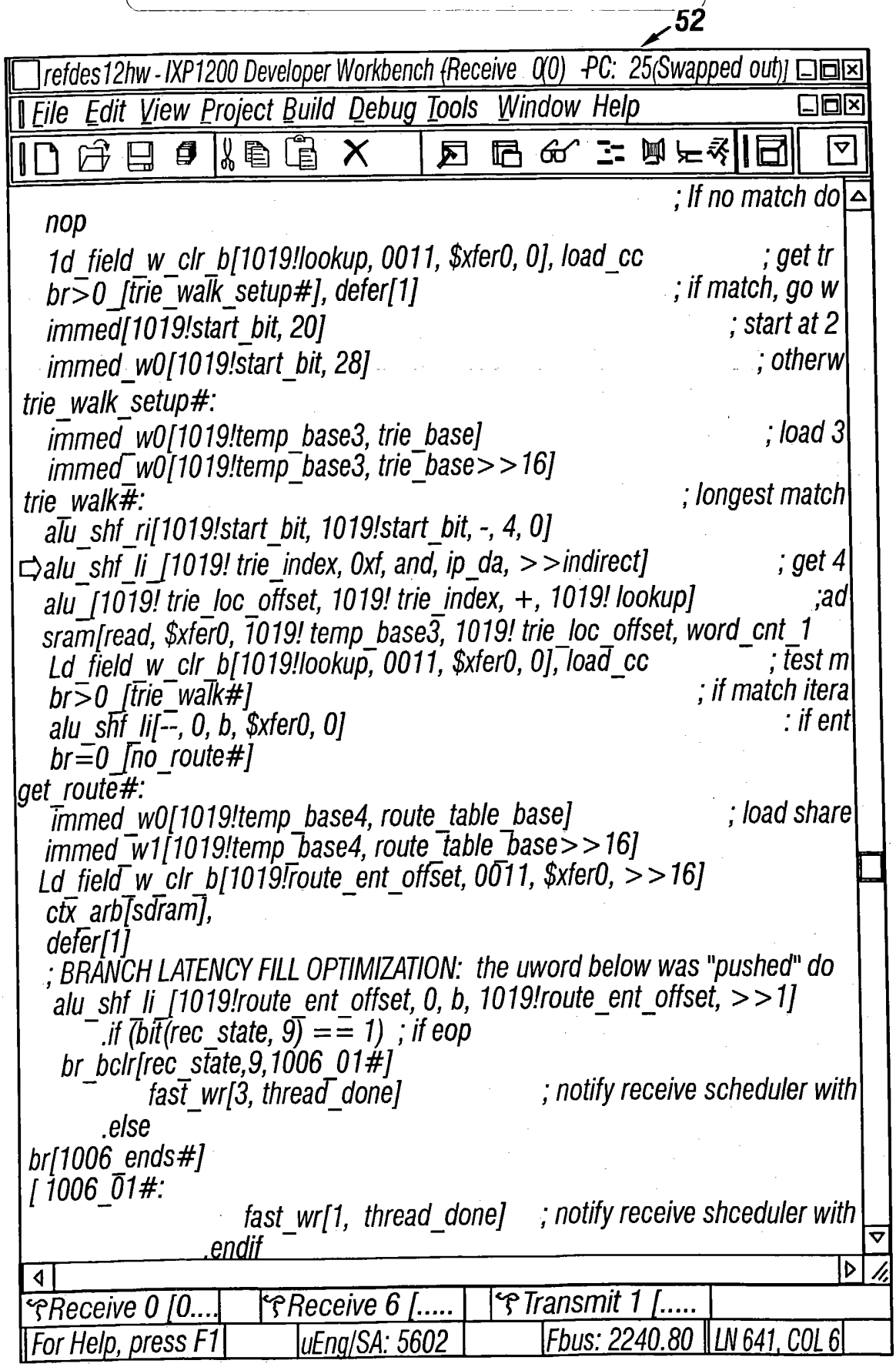
52
refdes12hw - IXP1200 Developer Workbench (Receive 0(0) PC: 25(Swapped out))
File Edit View Project Build Debug Tools Window Help
; If no match do
nop
1d_field_w_clr_b[1019!lookup, 0011, $xfer0, 0], load_cc ; get tr
br>0_[trie_walk_setup#], defer[1] ; if match, go w
immed[1019!start_bit, 20] ; start at 2
immed_w0[1019!start_bit, 28] ; otherw
trie_walk_setup#:
immed_w0[1019!temp_base3, trie_base] ; load 3
immed_w0[1019!temp_base3, trie_base>>16]
trie_walk#: ; longest match
alu_shf_ri[1019!start_bit, 1019!start_bit, -, 4, 0]
alu_shf_li_[1019! trie_index, 0xf, and, ip_da, >>indirect] ; get 4
alu_[1019! trie_loc_offset, 1019! trie_index, +, 1019! lookup] ;ad
sram[read, $xfer0, 1019! temp_base3, 1019! trie_loc_offset, word_cnt_1
Ld_field_w_clr_b[1019!lookup, 0011, $xfer0, 0], load_cc ; test m
br>0_[trie_walk#] ; if match itera
alu_shf_li[--, 0, b, $xfer0, 0] : if ent
br=0_[no_route#]
get_route#:
immed_w0[1019!temp_base4, route_table_base] ; load share
immed_w1[1019!temp_base4, route_table_base>>16]
Ld_field_w_clr_b[1019!route_ent_offset, 0011, $xfer0, >>16]
ctx_arb[sdram],
defer[1]
; BRANCH LATENCY FILL OPTIMIZATION: the uword below was "pushed" do
alu_shf_li_[1019!route_ent_offset, 0, b, 1019!route_ent_offset, >>1]
.if (bit(rec_state, 9) == 1) ; if eop
br_bclr[rec_state,9,1006_01#]
fast_wr[3, thread_done] ; notify receive scheduler with
.else
br[1006_ends#]
[ 1006_01#:
fast_wr[1, thread_done] ; notify receive shceduler with
.endif
Receive 0 [0....
Receive 6 [.....
Transmit 1 [.....
For Help, press F1
uEng/SA: 5602
Fbus: 2240.80
LN 641, COL 6

FIG. 15

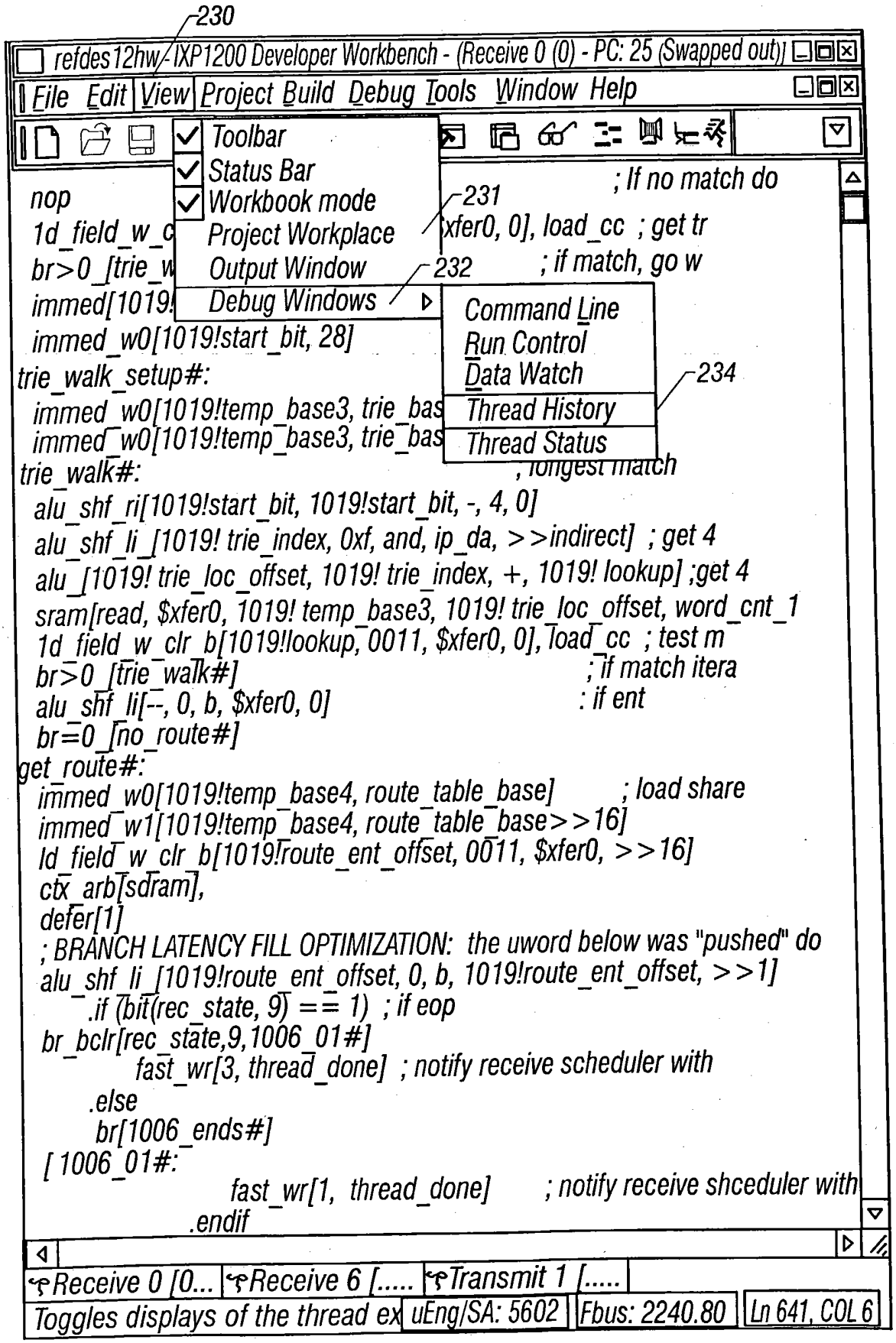
230
refdes12hw - IXP1200 Developer Workbench - (Receive 0 (0) - PC: 25 (Swapped out))
File Edit View Project Build Debug Tools Window Help
Toolbar
Status Bar
Workbook mode
Project Workplace
Output Window
Debug Windows
231
232
Command Line
Run Control
Data Watch
Thread History
Thread Status
234
nop
1d_field_w_c
br>0 [trie_w
immed[1019!
immed_w0[1019!start_bit, 28]
trie_walk_setup#:
immed_w0[1019!temp_base3, trie_bas
immed_w0[1019!temp_base3, trie_bas
trie_walk#:
alu_shf_ri[1019!start_bit, 1019!start_bit, -, 4, 0]
alu_shf_li_[1019! trie_index, 0xf, and, ip_da, >>indirect] ; get 4
alu_[1019! trie_loc_offset, 1019! trie_index, +, 1019! lookup] ;get 4
sram[read, $xfer0, 1019! temp_base3, 1019! trie_loc_offset, word_cnt_1
1d_field_w_clr_b[1019!lookup, 0011, $xfer0, 0], load_cc ; test m
br>0 [trie_walk#]
alu_shf_li[--, 0, b, $xfer0, 0]
br=0 [no_route#]
get_route#:
immed_w0[1019!temp_base4, route_table_base]
immed_w1[1019!temp_base4, route_table_base>>16]
ld_field_w_clr_b[1019!route_ent_offset, 0011, $xfer0, >>16]
ctx_arb[sdram],
defer[1]
; BRANCH LATENCY FILL OPTIMIZATION: the uword below was "pushed" do
alu_shf_li_[1019!route_ent_offset, 0, b, 1019!route_ent_offset, >>1]
.if (bit(rec_state, 9) == 1) ; if eop
br_bclr[rec_state,9,1006_01#]
fast_wr[3, thread_done] ; notify receive scheduler with
.else
br[1006_ends#]
[ 1006_01#:
fast_wr[1, thread_done] ; notify receive shceduler with
.endif
; If no match do
xfer0, 0], load_cc ; get tr
; if match, go w
; longest match
; if match itera
: if ent
Receive 0 [0...
Receive 6 [.....
Transmit 1 [.....
Toggles displays of the thread ex
uEng/SA: 5602
Fbus: 2240.80
Ln 641, COL 6

FIG. 16

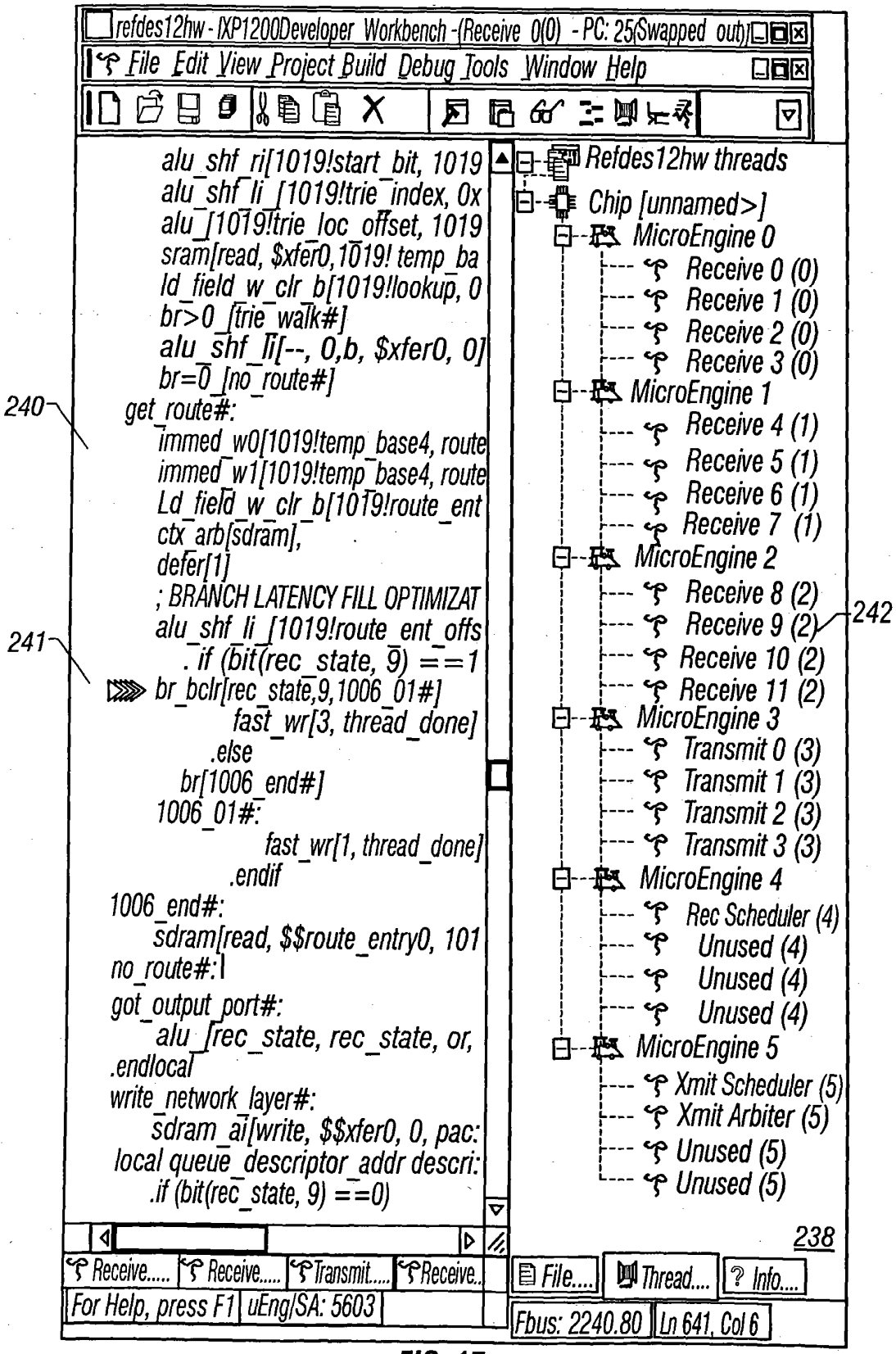
refdes12hw - IXP1200Developer Workbench - [Receive 0(0) - PC: 25 (Swapped out)]
File Edit View Project Build Debug Tools Window Help
alu_shf_ri[1019!start_bit, 1019
alu_shf_li_[1019!trie_index, 0x
alu_[1019!trie_loc_offset, 1019
sram[read, $xfer0,1019! temp_ba
ld_field_w_clr_b[1019!lookup, 0
br>0_[trie_walk#]
alu_shf_li[--, 0,b, $xfer0, 0]
br=0_[no_route#]
get_route#:
immed_w0[1019!temp_base4, route
immed_w1[1019!temp_base4, route
Ld_field_w_clr_b[1019!route_ent
ctx_arb[sdram],
defer[1]
; BRANCH LATENCY FILL OPTIMIZAT
alu_shf_li_[1019!route_ent_offs
. if (bit(rec_state, 9) ==1
br_bclr[rec_state,9,1006_01#]
fast_wr[3, thread_done]
.else
br[1006_end#]
1006_01#:
fast_wr[1, thread_done]
.endif
1006_end#:
sdram[read, $$route_entry0, 101
no_route#:
got_output_port#:
alu_[rec_state, rec_state, or,
.endlocal
write_network_layer#:
sdram_ai[write, $$xfer0, 0, pac:
local queue_descriptor_addr descri:
.if (bit(rec_state, 9) ==0)
240
241
Refdes12hw threads
Chip [unnamed>]
MicroEngine 0
Receive 0 (0)
Receive 1 (0)
Receive 2 (0)
Receive 3 (0)
MicroEngine 1
Receive 4 (1)
Receive 5 (1)
Receive 6 (1)
Receive 7 (1)
MicroEngine 2
Receive 8 (2)
Receive 9 (2)
Receive 10 (2)
Receive 11 (2)
242
MicroEngine 3
Transmit 0 (3)
Transmit 1 (3)
Transmit 2 (3)
Transmit 3 (3)
MicroEngine 4
Rec Scheduler (4)
Unused (4)
Unused (4)
Unused (4)
MicroEngine 5
Xmit Scheduler (5)
Xmit Arbiter (5)
Unused (5)
Unused (5)
238
Receive..... Receive..... Transmit..... Receive...
File.... Thread.... Info....
For Help, press F1 uEng/SA: 5603
Fbus: 2240.80 Ln 641, Col 6

FIG. 17

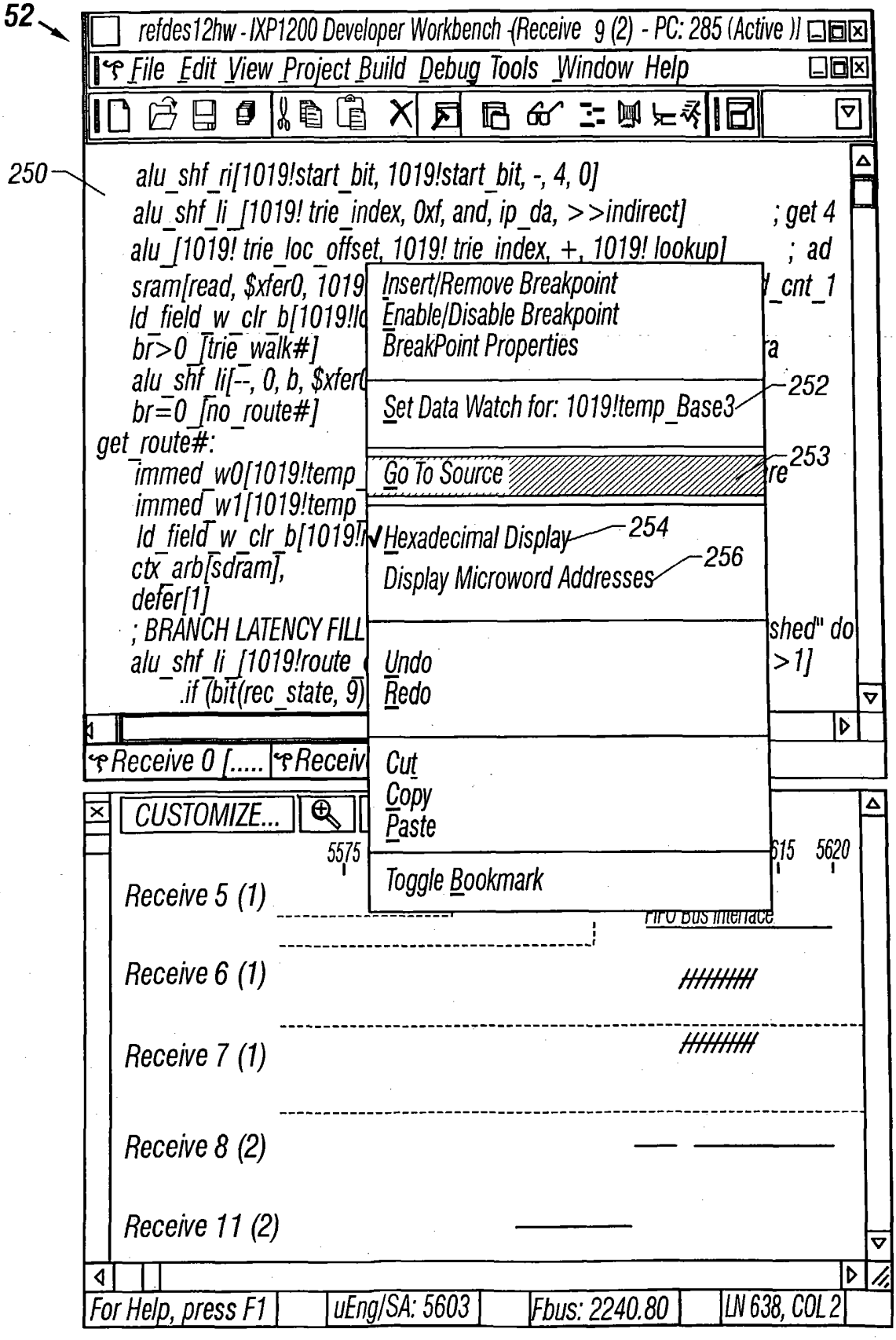
52
refdes12hw - IXP1200 Developer Workbench -(Receive 9 (2) - PC: 285 (Active ))
File Edit View Project Build Debug Tools Window Help
250
alu_shf_ri[1019!start_bit, 1019!start_bit, -, 4, 0]
alu_shf_li_[1019! trie_index, 0xf, and, ip_da, >>indirect] ; get 4
alu_[1019! trie_loc_offset, 1019! trie_index, +, 1019! lookup] ; ad
sram[read, $xfer0, 1019
ld_field_w_clr_b[1019!lc
br>0 [trie_walk#]
alu_shf_li[--, 0, b, $xfer
br=0 [no_route#]
get_route#:
immed_w0[1019!temp_
immed_w1[1019!temp
ld_field_w_clr_b[1019!
ctx_arb[sdram],
defer[1]
; BRANCH LATENCY FILL
alu_shf_li_[1019!route_
.if (bit(rec_state, 9)
Insert/Remove Breakpoint
Enable/Disable Breakpoint
BreakPoint Properties
Set Data Watch for: 1019!temp_Base3
252
Go To Source
253
Hexadecimal Display
254
Display Microword Addresses
256
Undo
Redo
Cut
Copy
Paste
Toggle Bookmark
Receive 0 [.....
Receiv
CUSTOMIZE...
5575
5615
5620
Receive 5 (1)
FIFO Bus Interface
Receive 6 (1)
Receive 7 (1)
Receive 8 (2)
Receive 11 (2)
For Help, press F1
uEng/SA: 5603
Fbus: 2240.80
LN 638, COL 2

FIG. 18

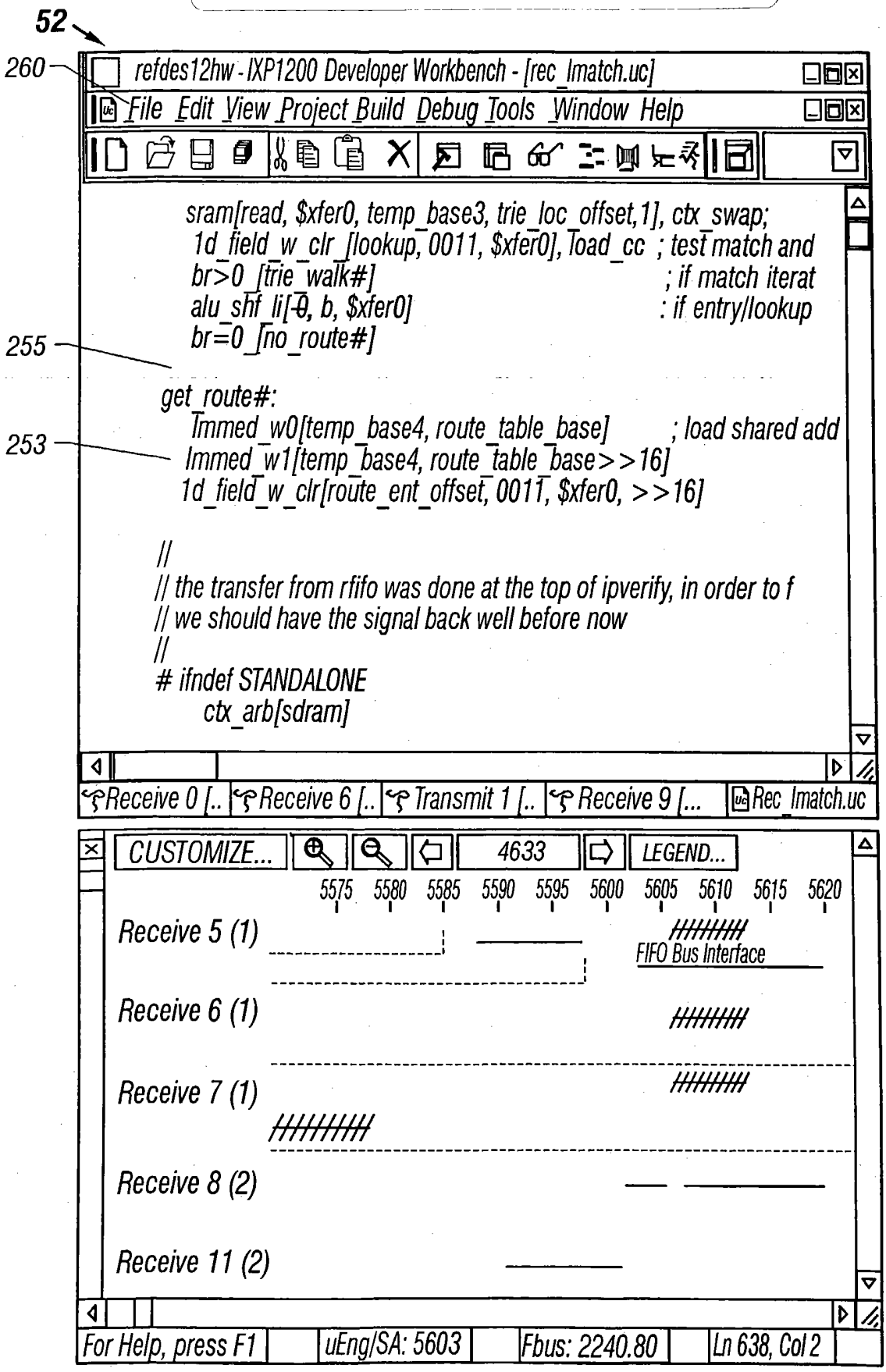
52
260
refdes12hw - IXP1200 Developer Workbench - [rec_lmatch.uc]
File Edit View Project Build Debug Tools Window Help
sram[read, $xfer0, temp_base3, trie_loc_offset,1], ctx_swap;
1d_field_w_clr_[lookup, 0011, $xfer0], load_cc ; test match and
br>0_[trie_walk#] ; if match iterat
alu_shf_li[0, b, $xfer0] : if entry/lookup
255
br=0_[no_route#]
get_route#:
253
Immed_w0[temp_base4, route_table_base] ; load shared add
Immed_w1[temp_base4, route_table_base>>16]
1d_field_w_clr[route_ent_offset, 0011, $xfer0, >>16]
//
// the transfer from rfifo was done at the top of ipverify, in order to f
// we should have the signal back well before now
//
# ifndef STANDALONE
ctx_arb[sdram]
Receive 0 [..
Receive 6 [..
Transmit 1 [..
Receive 9 [...
Rec_lmatch.uc
CUSTOMIZE...
4633
LEGEND...
5575 5580 5585 5590 5595 5600 5605 5610 5615 5620
Receive 5 (1)
FIFO Bus Interface
Receive 6 (1)
Receive 7 (1)
Receive 8 (2)
Receive 11 (2)
For Help, press F1
uEng/SA: 5603
Fbus: 2240.80
Ln 638, Col 2

FIG. 19